New 110 dB, 10 MHz to 8 GHz, Electronic Step Attenuator for Fast-Switching Microwave Signal Generators

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Introduction

A step attenuator finds wide-spread usage as a means of accurately extending the attenuation range of test and measurement instruments. A typical application would be to extend the output amplitude range of a microwave signal generator. Often an amplitude control loop can accurately set the power or gain level over three or four decades of range, but frequently this is not enough range. Historically, the mechanical step attenuator has been the preferred solution. This device is composed of cells, each having a pair of single-throw, double-pole mechanical switches. Between one pair of switch throw positions is a low-loss through path. Between the alternate pair of throw positions is a precision attenuator. By cascading three or four cells, precision "steps" of attenuation can be switched in or out. A common arrangement includes a 10 dB, 20 dB, and two 40 dB cells. By switching different combinations of cells, 10 dB steps from zero to 110 dB can be had. Since an ALC or AGC network can easily adjust itself over a 10 dB range, it is now possible to continuously adjust power or gain over a 110 dB range.

The mechanical step attenuator is still an appropriate choice where the lowest insertion loss in the "0 dB" state is necessary, or where any degradation in linearity performance is unacceptable. That said, there are drawbacks with a mechanical attenuator. By its very nature, it is prone to mechanical fatigue, and ultimately failure. A great deal of materials and process engineering is dedicated to the high reliability devices found in many of today's microwave test equipment. The Engineering and Manufacturing costs for these devices are not insubstantial; and it is not unusual to see prices for the highest performance models to top $4,000.

Another inherent drawback for the mechanical step attenuator is the time it takes for the signal amplitude level to settle to its final value. The mechanical switch is spring-loaded, and as such is subject to "chatter", or it experiences the intermittent closing and opening of the switch as it changes state. Typically, this time interval is measured in milliseconds, and is often specified in the 20 ms range for high performance mechanical step attenuators. However, once the mechanical switch is "closed", typically the amplitude settling occurs very quickly.

The electronic step attenuator, a relatively recent development, has another set of issues to contend with. Depending on the application, any of these issues could limit its usefulness for a given application. Among the issues:

1. Relatively high insertion loss
2. Relatively high Standing Wave Ratio (SWR)
3. Less linear performance (e.g. higher harmonic levels)
4. Higher continuous current draw (no mechanical latching mechanism)
5. More limited frequency range (related to first three issues)

An ideal step attenuator would have the best properties of both the mechanical and electronic versions. This would include low insertion loss, high return loss, high linearity, fast settling time, low power dissipation, and low cost of ownership (e.g. initial price, maintenance, calibration, and so forth). To that end, a new electronic attenuator has been developed with the intent to seek a compromise between the attributes of a mechanical and electronic attenuator. To do so required inventing a new way to use the latest state-of-the-art diode devices in a way not normally associated with the type of diode selected[1].

An example of the microwave signal generator applications that this attenuator is anticipated to address is the RFIC test, antenna test or signal simulation where fast switching speed of both frequency and amplitude are required. A traditional mechanical step attenuator would be un-usable, given the need for lowest test through-put time, and sheer number of RF level changes, i.e. switch state changes, required over the life of the test system. For this application, the key RF specifications for an electronic attenuator are:

Parameter	Unit	Spec Limit
Frequency Range		
Fmin	MHz	10[2]
Fmax	GHz	8
Attenuation Range (in 10 dB steps)	dB	110
Attenuation Flatness (over any 100 MHz BW)	dB	± 0.25
Maximum Input Power	dBm	30
Insertion Loss		
10 MHz	dB	10
1 GHz	dB	2.5
3 GHz	dB	7
8 GHz	dB	10
Harmonics (at +10 dBm input)	dBc	-57
Return Loss	dB	-8
Settling Time (to within 0.1 dB of final value)	µs	100

Table 1: Target Electrical Requirements

[1] U.S. Patent 7,639,100
[2] Usable down to 4 MHz

Electrical Design Approach

There are essentially two approaches to the design of the switches in an electronic step attenuator. FET devices, with the RF signal traversing the drain-source channel, can be switched by biasing the gate for a conductive or pinched-off channel. FET devices have potential drawbacks with insertion loss and linearity, particularly at the proposed lower RF frequency range of this attenuator. Short lifetime P-I-N diodes may also have the same limitations as the FET devices; albeit, for different reasons. Long lifetime P-I-N diodes, such as those traditionally used for continuously variable attenuators, generally have more insertion loss than typically found with either FET devices or short lifetime P-I-N diodes, but do not suffer carrier re-combination in the intrinsic region at lower frequencies. For this reason, long lifetime P-I-N diodes were chosen as the switching elements for this new electronic step attenuator.

To lessen the issue with insertion loss, the long lifetime P-I-N diodes have been used in parallel with each other to lessen the series resistance (R_S) of both the series and shunt diode elements for the switch. The drawback to this approach is that the capacitance of the diodes is increased with each parallel diode. The capacitance (C_T) limits the higher frequency performance for both insertion and return loss. By selecting diodes with very low capacitance, it was determined that the best compromise between reducing R_S and increasing C_T was with two parallel diodes for both the series and shunt diode switch elements. Furthermore, since the P-IN diodes are current controlled devices, it was found that the best compromise between minimizing current through each diode, and minimizing RF insertion loss was to drive each diode selected within a current range of 25 to 35 mA.

Once a P-I-N diode type was selected, a variation of the classic Spice diode model needed to be extracted. The variations to the classic Spice model for the diode affect the calculation of R_S and C_D. The details of the extraction of the polynomial coefficients for the C_D model are detailed elsewhere[3], and the R_S model coefficients were numerically extracted to match the published attenuation data for the diode. See Figure 1 for details of the Switch Diode Model.

Once the Diode Switch Model was extracted, electrical simulation using a non-linear model, and microwave analysis tool could be performed with ever-increasing complexity to include passive transition and discontinuity models created by E-M simulations of those elements as necessary. Particular attention was given to the thin-film attenuator elements, the T-junction discontinuities, and the mitered bends. Grounded coplanar waveguide was chosen as the transmission media as a compromise between optimizing for series or shunt component placement.

[3] Non-Linear Capacitance Model (white paper), 21 October 2005, C. Fuentes - reference Appendix A

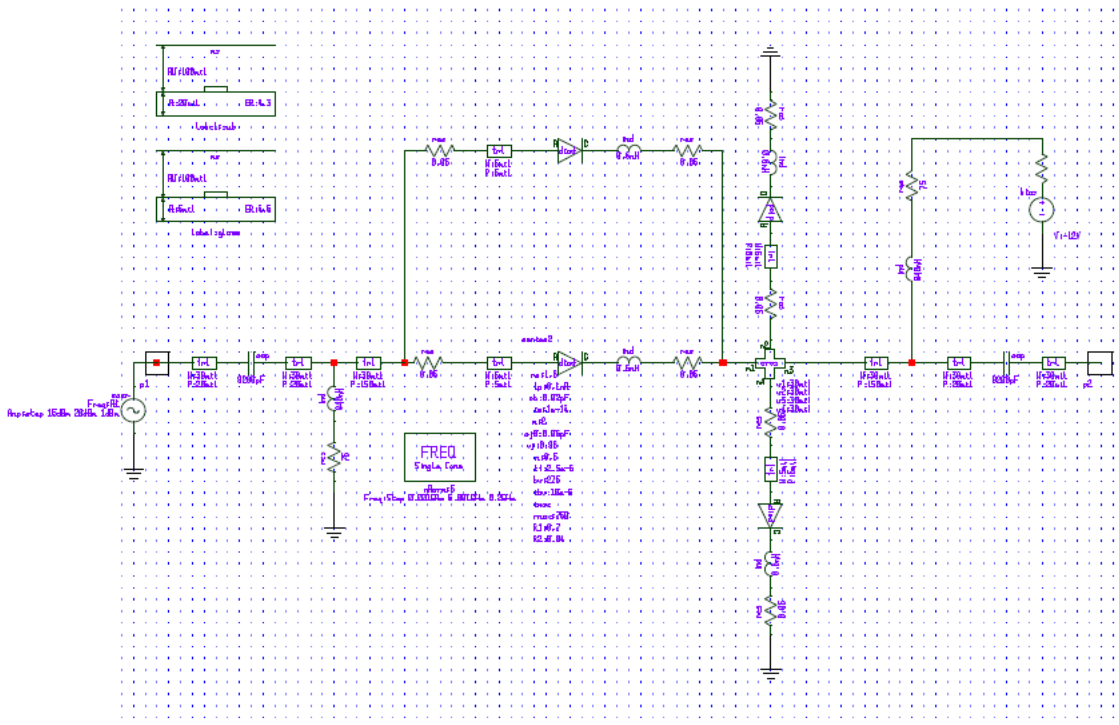


Figure 1: Series-Shunt Switch Model with P-I-N Diodes

The physical transmission line media itself was given significant consideration. Two possible choices are between a soft plastic substrate such as Duroid®, and a hard ceramic substrate such as alumina (Al_2O_3) or Aluminum-Nitride. The hard substrates allow better precision etching of the transmission lines, and Al-N also has a superior thermal conductivity compared to most transmission media. Nevertheless, one limitation with using any hard substrate is the substrates themselves must be a rectilinear shape for reasonable cost-effectiveness.

It is possible to laser scribe a hard substrate into a non-rectilinear shape; however, an entire wafer is usually consumed in the process (cost: between $400 to $1000, depending on size and material). Furthermore the complex geometry laser scribed substrates tend to be very fragile, and consequently difficult to handle. To piece together a relatively large circuit out of rectilinear shapes would require a significant number of wire-bond transitions between concatenations of these substrates. Even with a 30 dB return-loss per transition, a relatively small number (≥ 12) of transitions would prohibit meeting an overall 10 dB return loss for the assembly.

Furthermore, the hard ceramic substrates tend to have a higher relative dielectric constant, compared with the soft substrates. The higher dielectric constant increases the parasitic shunt capacitance of the series diode elements in the switch, limiting the high frequency insertion and return loss performance. For these reasons, a soft substrate material was chosen for this design, except for the actual attenuator circuits themselves.

The plating for the transmission line has also been given some consideration. Ideally, the highest conductivity plating, silver plating, would allow the lowest possible losses due to conductivity issues. The silver plating process that allows a reasonably thick plate to be applied is an electroplating process that requires the circuits to be completely continuous. Unfortunately, this is not an easily met condition considering that there are DC blocks required to keep DC current out of the resistive elements of the attenuators. There are ways around this problem, but they require manual handling processes that are not conducive to consistent process control. Furthermore, it is expected that gold wire bonding will be required to transition from the Duroid® substrate to the precision thin-film attenuator circuits. A standard electroless gold plating process was used for the soft substrates.

The types of the attenuator circuits were also given some consideration. It is impractical to fabricate a 40 dB attenuator chip directly; the series resistance values for either a T- or Pi attenuator are too large for either 50 Ω or 100 Ω per square materials. The higher valued Ohm per square materials causes the fabrication of the shunt resistors equally impractical. High attenuation value chip attenuators typically require multiple metal deposition and etch-back processes, raising the cost considerably. A 20 dB attenuator is practical to fabricate; however after much simulation, it appears that the return loss of a 20 dB attenuator is still significantly worse than a 10 dB attenuator, or even a set of 10 dB attenuators. It also became an advantage to distribute the attenuation across a longer electrical length, so that between each switch there was at least half of a guided wavelength at the highest specified operating frequency[4]. Figure 2 depicts the details of the RF layout for a single attenuator cell.

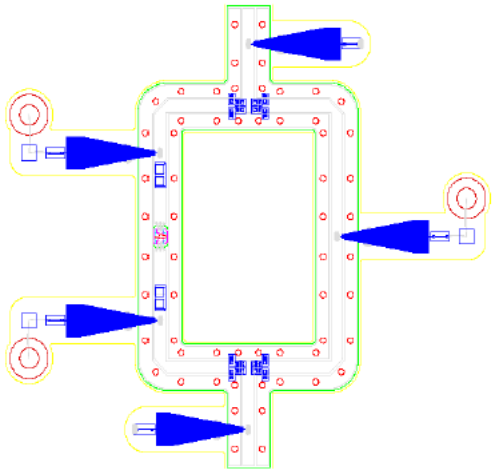


Figure 2: 10 dB "Cell" RF Layout

[4] It is assumed that the lowest waveguide index, TE_{10} would be the dominant induced waveguide mode. For that mode, there is approximately $54.57*\nu[1-(\lambda/\lambda c)^2]$ dB of attenuation for an evanescent propagation mode. For more information, please refer to the *Waveguide Handbook*, by N. Marcuvitz.

Mechanical Design Approach

A number of issues, particularly providing high degrees of electrical isolation, provided the pretext for reconsidering using standard mechanical microcircuit design practices. For example, rather than using a relatively thin conductive gasket, a much thicker RF absorbing gasket has been used for this design. The thick gasket allowed the RF channels to be made smaller, without causing a mechanical interference problem with new, much larger conical coils. Large RF filter feedthrus are used, rather than the capacitive-only feedthrus. The lids over the RF section and controller PCA are fabricated from cold rolled steel for superior attenuation of radiated energy generated from the switching power supply. The microcircuit body is fabricated from aluminum, with a relatively thick silver plate coating. The silver plating is to help reduce conductivity losses that may adversely affect RF insertion loss. See Figure 3 below for the mechanical structure.

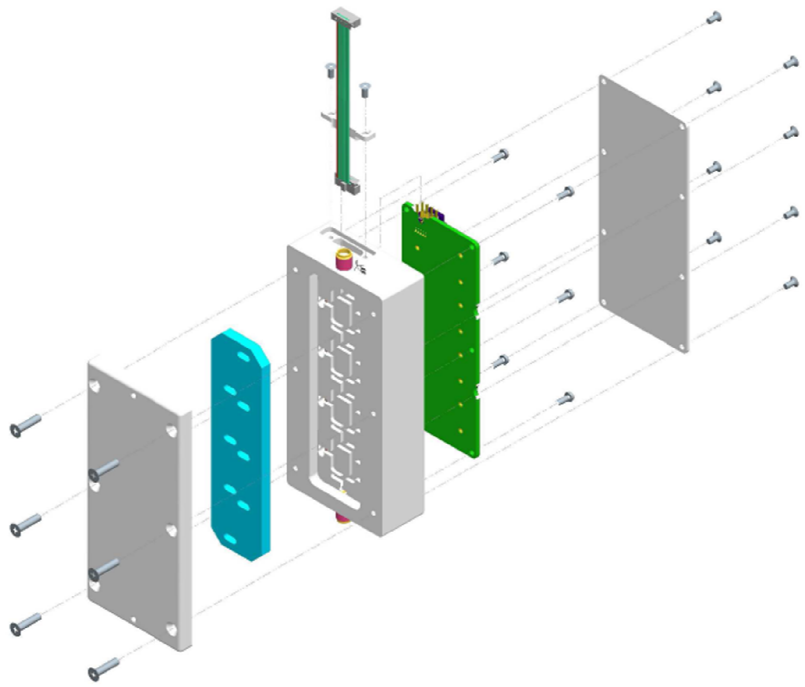


Figure 3: Exploded Mechanical View of Electronic Attenuator

Simulation Results

Three different attenuator cells were simulated from the individual switch and attenuator circuits that were discussed earlier. The attenuation values of these cells are 10, 20, and 40 dB. To create a 110 dB attenuator requires one 10 dB, one 20 dB, and two 40 dB cells. The 10 dB and 20 dB cells are closest to the RF input and RF output connectors respectively. The 10 dB cell has the best return loss. Each cell has been simulated for insertion loss and return loss in the "through" and attenuation states. Each cell has also been simulated for harmonic generation with an input of +10 dBm at the extreme ends of the frequency range (10 MHz and 8 GHz); it is assumed that a signal generator of sufficient quality would have harmonics at or below the level specified for the electronic attenuator.

RF Simulation: The following plots show simulated performance for insertion loss, return loss, and spectral content for the 10 dB cell in its "through" and attenuation states. The simulations confirm the key specifications given in Table 1. Simulations for the 20 dB and 40 dB cells are very similar. The spectral content is not strongly affected with or without the thin-film attenuator; it is largely dependent on the current bias of the P-I-N diodes in the switching elements. The simulation was conducted with the diodes drawing 25 mA at 25 °C.

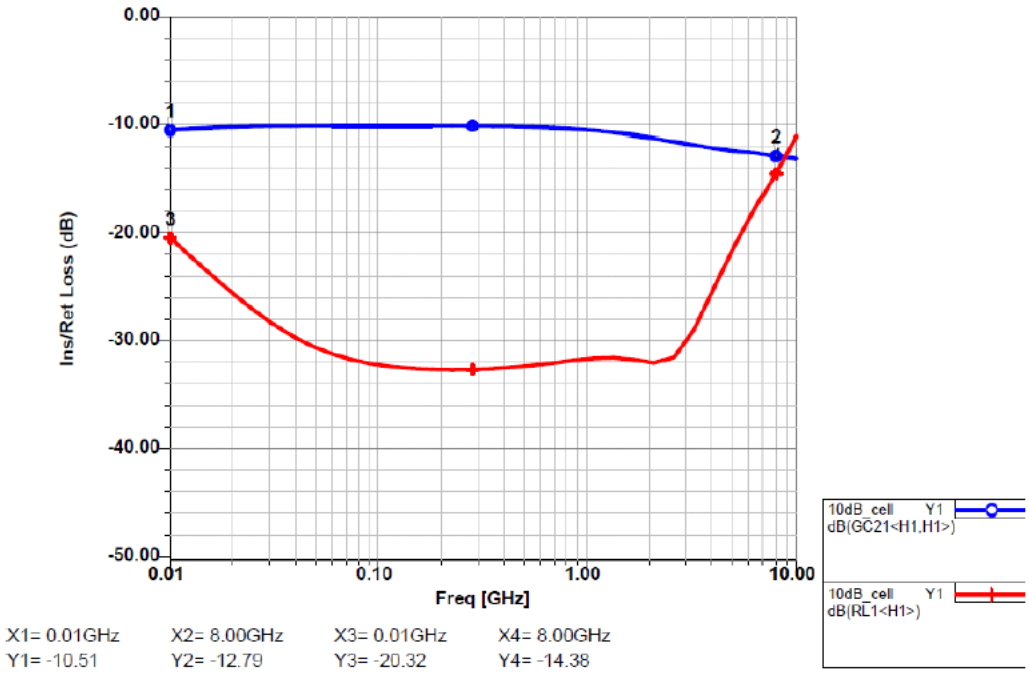


Figure 4: 10 dB "Cell" Insertion and Return Loss in Attenuation State

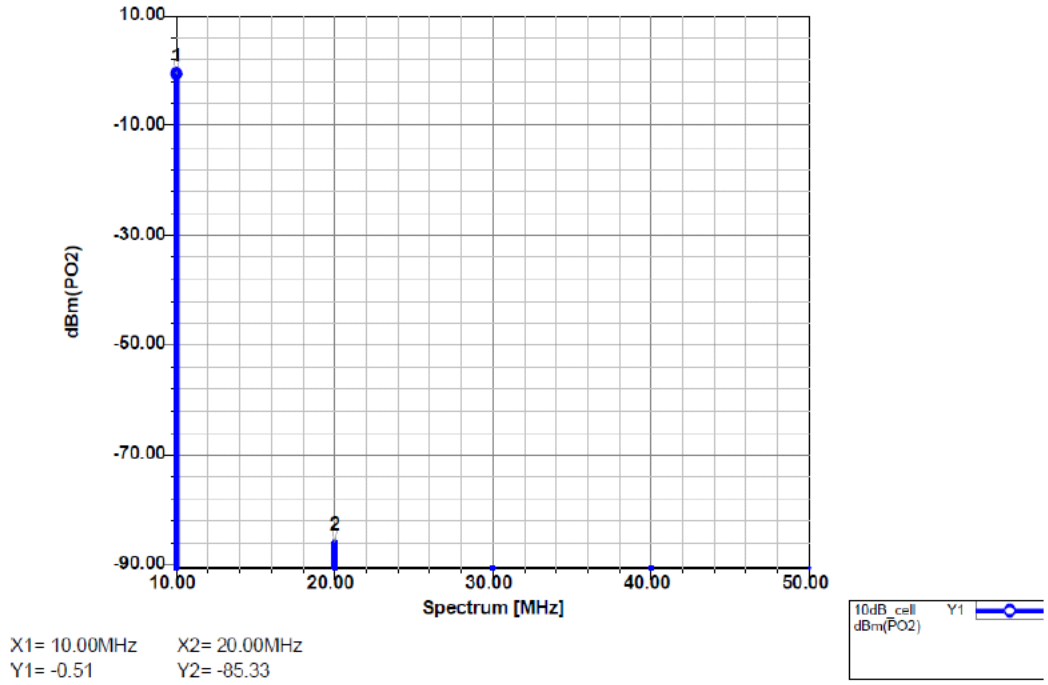


Figure 5: 10 dB "Cell" Spectral Output at 10 MHz in Attenuation State

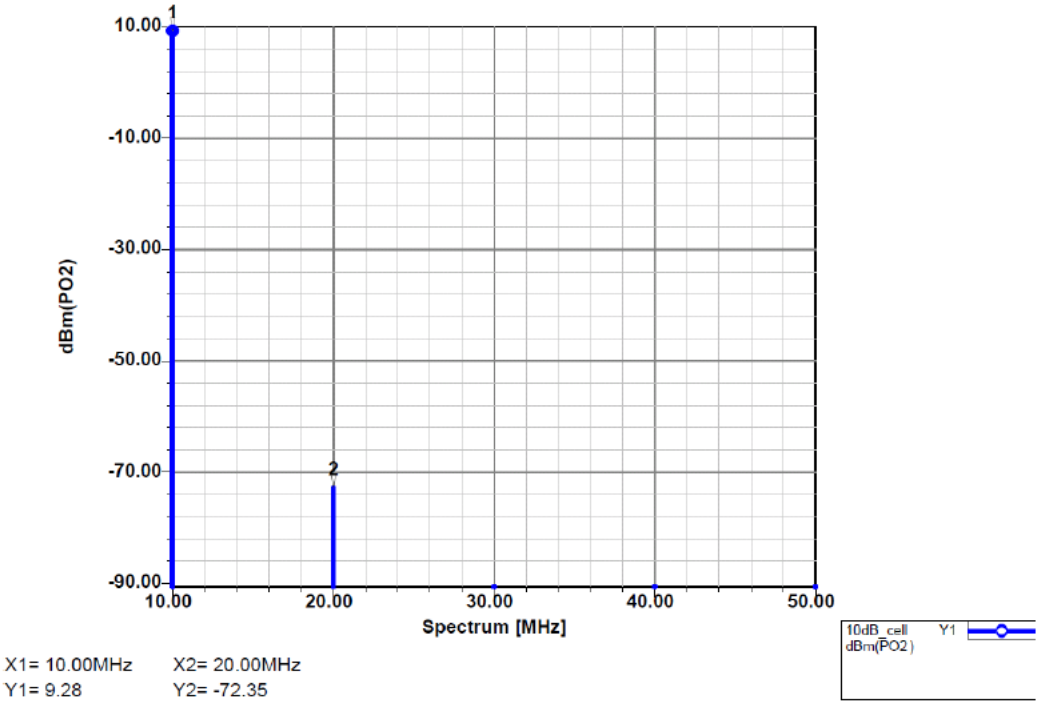


Figure 6: 10 dB "Cell" Spectral Output at 10 MHz in "Through" State

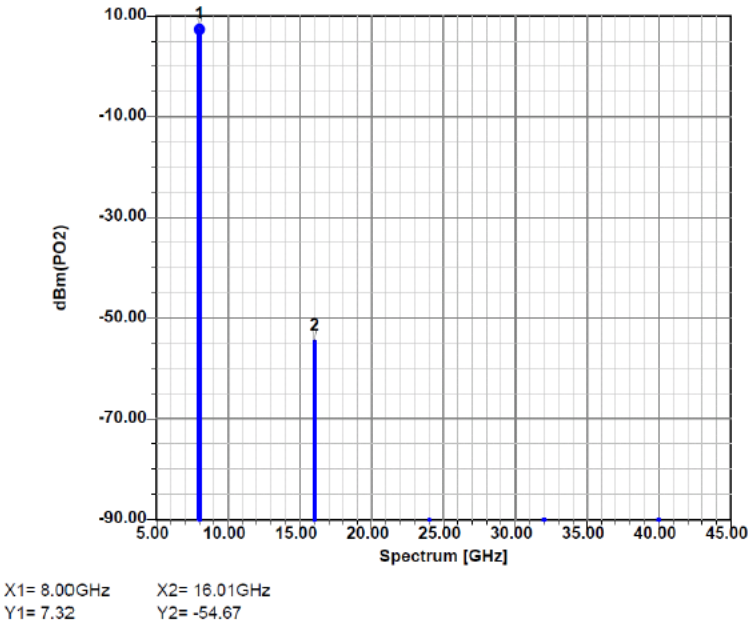


Figure 7: 10 dB "Cell" Spectral Output at 8 GHz in "Through" State

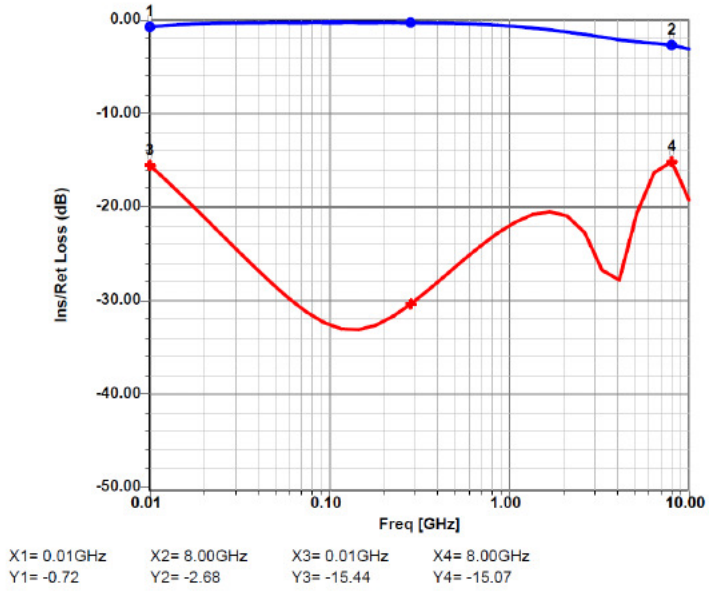


Figure 8: 10 dB "Cell" Insertion and Return Loss in "Through" State

Analog Simulation: An interface for the electronic step attenuator needs to be provided that as closely as possible resembles those for the mechanical step attenuators to allow the electronic attenuator to be used as a drop-in replacement for the mechanical step attenuator in various applications. There are some attributes of a mechanical step attenuator that will be difficult to replicate, such as the current shut-off mechanism after switching states. The electronic step attenuator requires continuous current draw to maintain a switched state.

For the electronic step attenuator, a pull-up resistor is used on the analog control lines[5] to provide a logic level suitable for controlling the analog switches that drive the P-I-N diodes within the RF switches. The series P-I-N diodes within a RF switch are conducting when a -12 Volt supply drives 25 mA of current through each diode. The shunt diodes are back-biased with this bias condition, thus drawing very little current. The shunt diodes conduct with a +5 Volt bias driving 25 mA through each diode, while the series diodes are back-biased. In any given state for the entire attenuator, half of the overall series diodes are turned-on, and half are turned-off. Similarly, the shunt diodes are half-on, half-off. There are a total of 64 P-I-N diodes for the four cell step attenuator, so on each voltage supply at any given time there is approximately 400 mA of current drawn. Since only a positive supply is made available for the mechanical step attenuator, the negative voltage supply needs to be created from the positive supply voltage. This is accomplished with a switching power supply, using one of the inverting topologies. The switching frequency was selected to allow relatively easy filtering on both the input and output of the new negative voltage supply.

To help insure that the analog control circuitry would behave as expected, the original driver circuitry for the mechanical step attenuator has been included in the simulation, along with the new analog switches that will be used on the electronic step attenuator control PCA. Unfortunately, there is not an exact model for the analog switch used for this design; however, there was a model that is relatively close. The MOSFET R_{DS} for the switch device model is somewhat higher than the actual device. This was partially compensated for by reducing the load resistance, allowing 50 mA (current for two parallel P-I-N diodes) to flow across the FET. Based on this model, it was possible to switch attenuator states in up to 1 µs. This is as fast as almost any programmable source can change frequency or power level states.

The simulation for the switching regulator provided some insight into what trade-offs can be made to supply the 400 mA from a -12 Volt supply. Two different switching regulators were tried, with different combinations of transformers and filtering circuits. The higher switching frequency design with the smaller transformer appears to be the more robust design from the standpoint of tolerating a lower input supply voltage and more current supply headroom.

For integration of the electronic attenuator within a larger system, it may be important to anticipate the switching regulator noise spectral content as well as noise amplitude levels. The following diagrams (See Figures 9, 10 and 11) depict the switching regulator topology, and the simulation results for the switching regulator.

[5] The analog control takes the form of an open-collector or ground.

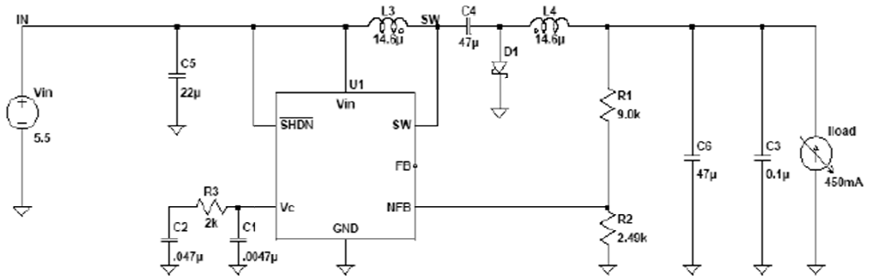


Figure 9: Switching Regulator Schematic

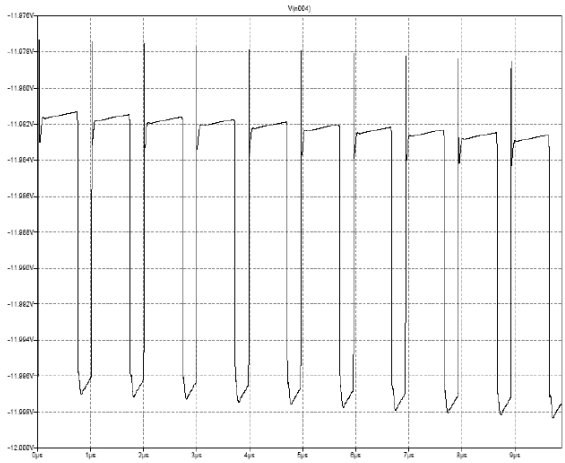


Figure 10: Switching Regulator Steady State Time Domain Output Waveform

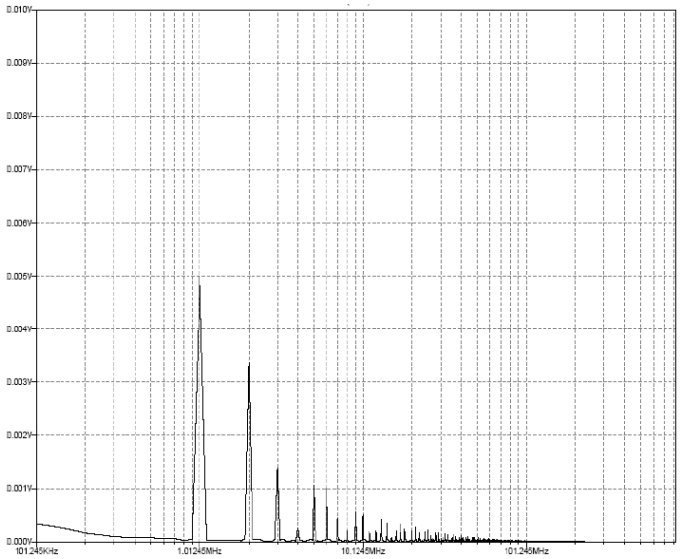


Figure 11: FFT Transform of Steady State Output

Test Data

Comprehensive RF Testing has been conducted to validate the design goals. Prototype units have been tested for a wide range of RF parameters. Pre-production units have been tested for more extensively for insertion loss, return loss, and harmonic generation. The production goal is to meet a three sigma requirement. Refer to Table 2 for pre-production test data, and statistical results.

The parameters tested for, and presented in figures to follow, are:

1. "0 dB" Insertion Loss: a maximum of -10 dB, with a nominal value of 8 dB at 8 GHz
2. Return Loss: a maximum of -8 dB, with a nominal of -9.5 dB (2.0:1 SWR)
3. Harmonics: a maximum of -57 dBc, with a nominal of -60 dBc
4. Settling Time: a maximum of 100 µs, 40 µs nominally

Figures 13 and 15 depict data taken for a prototype and pre-production units respectively. As expected, the insertion loss at the maximum specified frequency, 8 GHz is at its peak value. Both the prototype and pre-production data indicate that the insertion loss is typically in the -7 to -9 dB range. This is consistent with a worst case expectation of -2.5 dB of loss per cell for a four cell design.

Figures 12 and 14 depict the prototype data taken for the Return Loss. The peak return loss of -9.4 dB is consistent with a cascade of four cells, each having a Return Loss of -21 dB, where the SWR peaks were co-incident. This would be difficult to judge from the simulation data; however, it does not seem unreasonable, given a typical cell return loss of -20 dB. The simulation data did not take into account the effects of the transition from the coplanar waveguide to coaxial input/output connectors either.

Figures 16 and 17 depict some of the prototype data taken for harmonic generation. As expected, the harmonics at the lower end of the frequency range tend to be worse than the harmonics at the upper end of the frequency range. This is an artifact of the carrier recombination issue within the intrinsic region of the P-I-N diodes. As the frequency approaches the lower end of the specified range, the diodes tend to behave more like rectifiers, rather than variable resistors. The simulation results are did not accurately predict the harmonic performance at the lower end of the specified frequency range; however, became more accurate for the upper end of the frequency range. This may be due to a poor estimate of the diode carrier recovery lifetime; this would be critical for simulating the low frequency performance, but less important for the high frequency performance.

Figure 18 depicts the settling time performance. The settling time is within the specified performance range. The settling time has been measured for single cell switching events, such as shown in the figure, and for multiple cells being switched simultaneously. Typically, the settling time is under 40 µs.

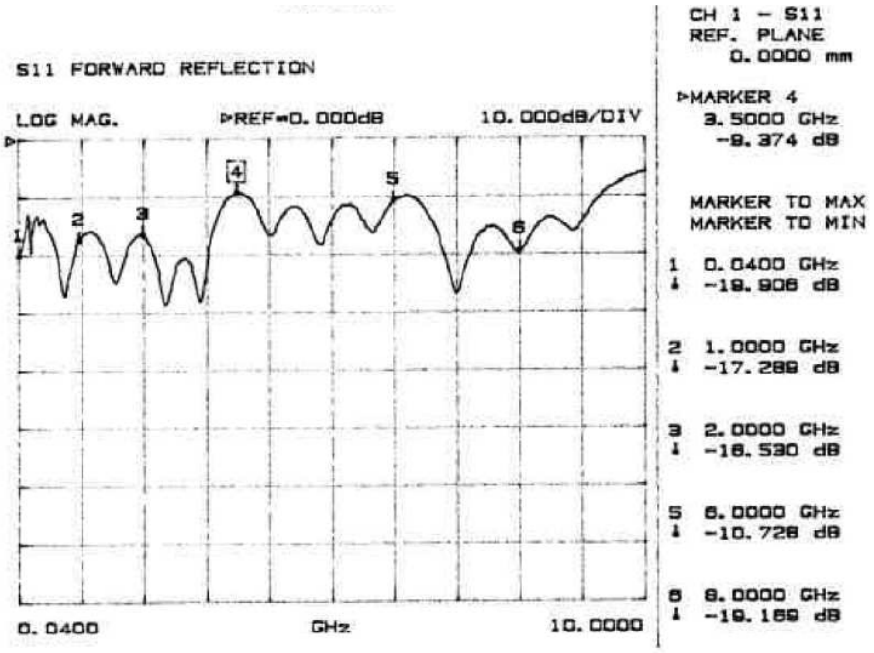


Figure 12: "0 dB" Return Loss in "Through" State

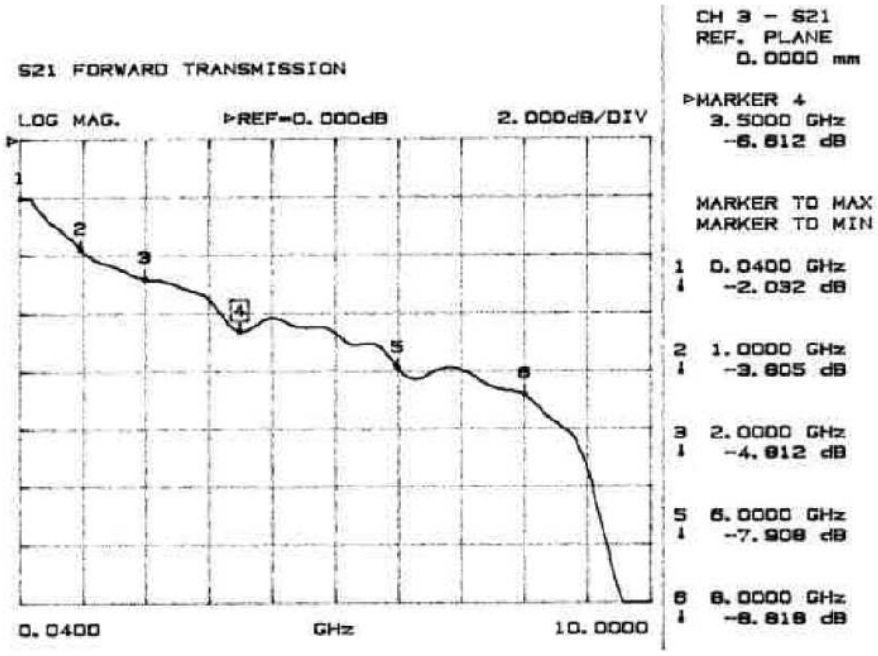


Figure 13: "0 dB" Insertion Loss in "Through" State

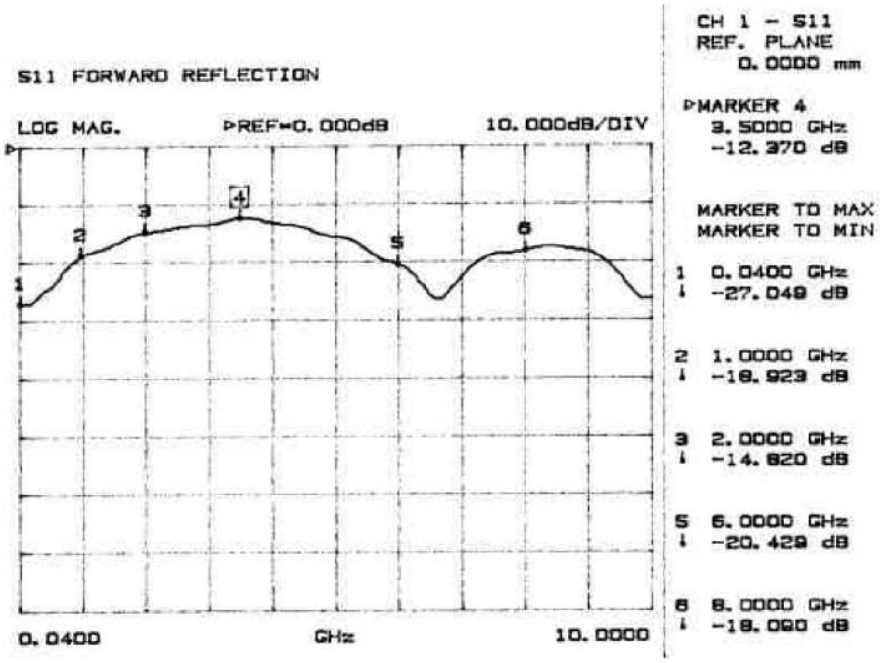


Figure 14: 10 dB Return Loss in Attenuation State

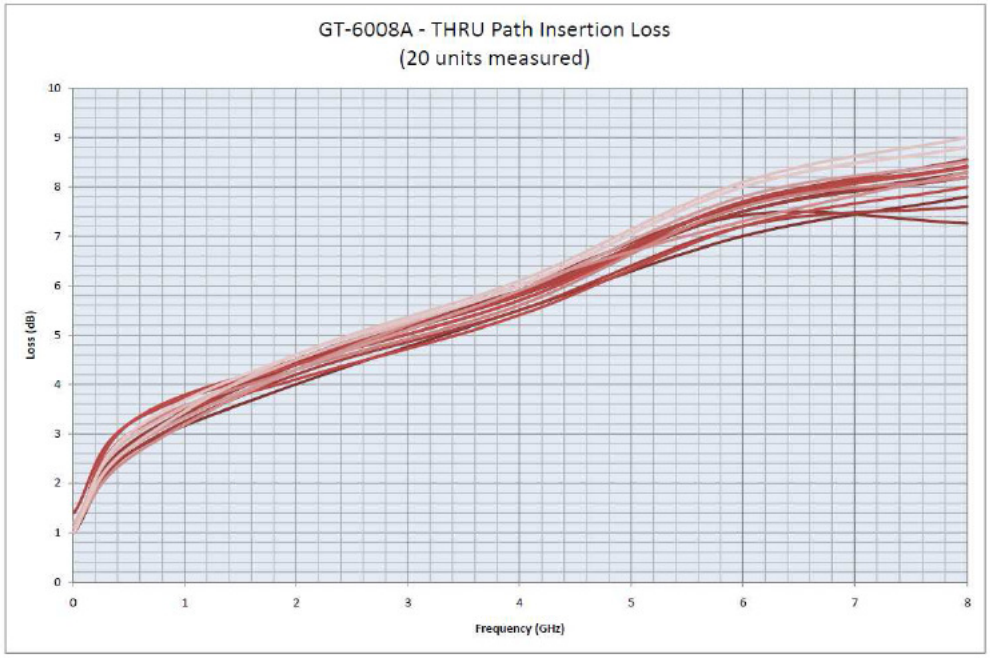


Figure 15: Attenuation Loss Tracking in "0 dB" State

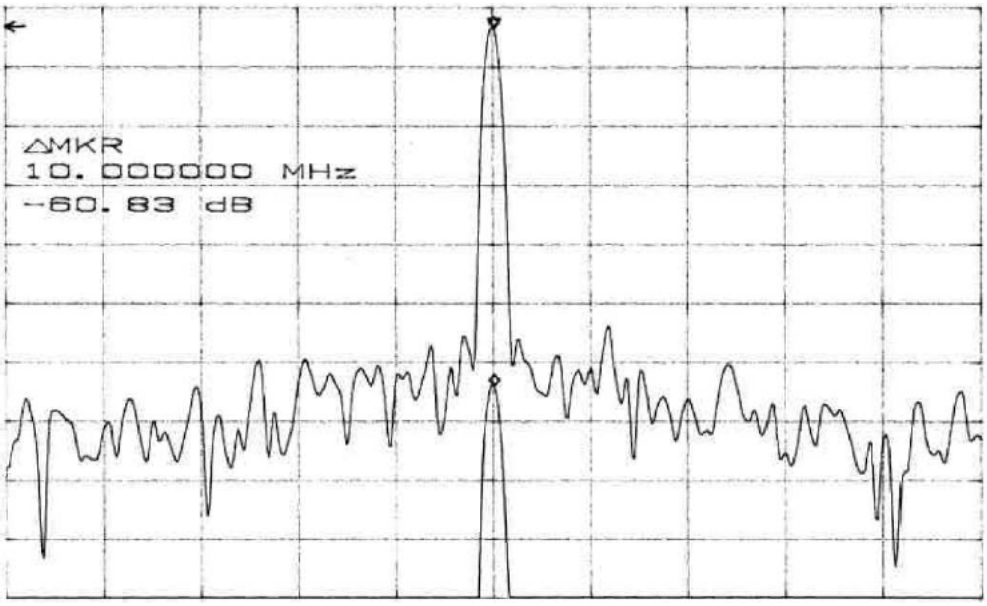


Figure 16: 10 MHz Fundamental Tone with 20 MHz Harmonic at +15 dBm Input Level

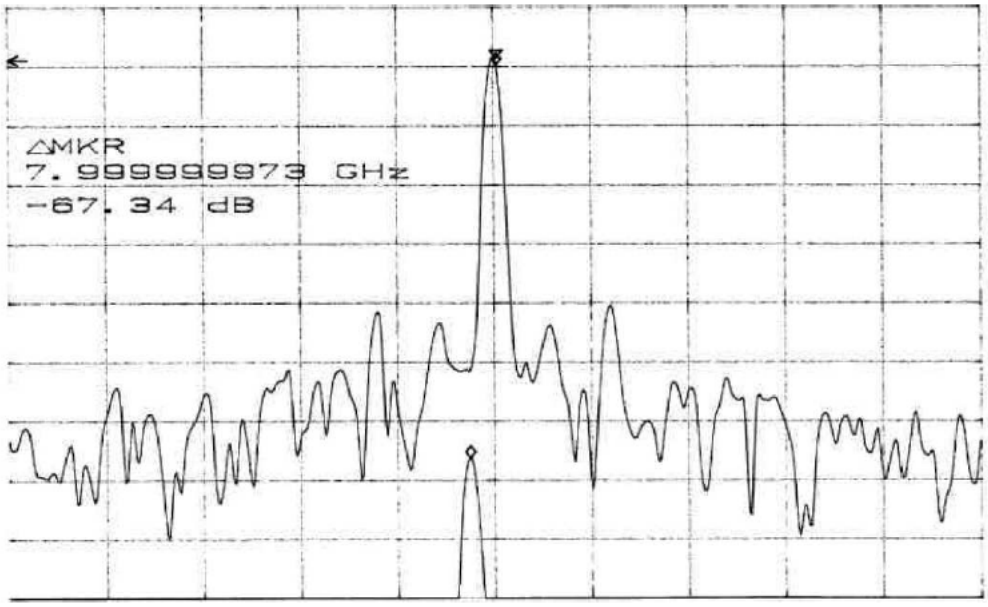
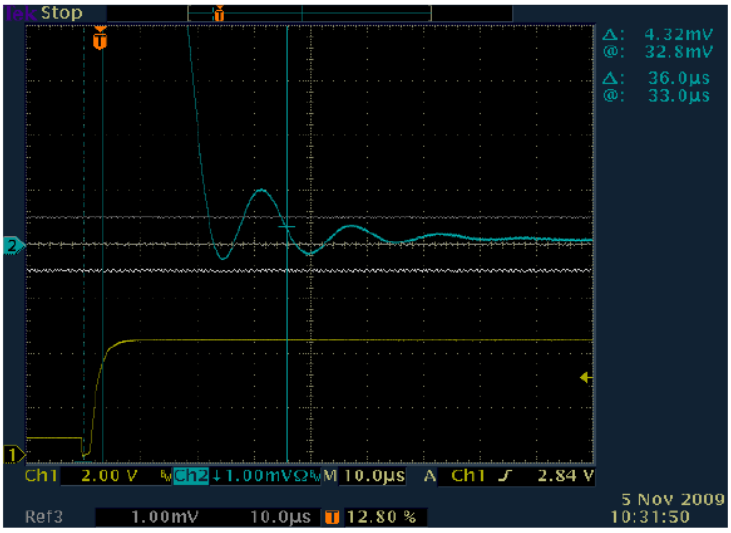


Figure 17: 8 GHz Fundamental Tone with 16 GHz Harmonic at +15 dBm Input Level



Frequency	1 GHz
Input Power	10 dBm
Switching From	10dB
Switching To	THRU
Settling to Within	0.1dB
Measured Settling Time	36 us

Figure 18: Amplitude Settling Time (Scale = 10 µs per division)

Parameter	Specification	Unit	Average	Standard Deviation
Insertion Loss at 10 MHz	-1.5 max	dB	-1.11	0.14
Insertion Loss at 8 GHz	-10 max	dB	-8.47	0.56
Return Loss at 8 GHz	-8.0 max	dB	-9.45	0.76
Harmonics at 10 MHz	-57 max.	dBc	-59.5	1.14
Harmonics at 8 GHz	-57 max.	dBc	-73.2	4.06

Table 2: Pre-Production Test Data Summary

Summary

A new 110 dB, 10 MHz to 8 GHz, electronic step attenuator for use with fast-switching microwave signal generators was developed using patented technology. The design method and test results were presented and the electronic step attenuator is available as an option in the Giga-tronics 2500B series of microwave signal generators.

Appendix A: Non-Linear Capacitance Coefficients Model

A more advanced model of the typical diode equation for junction capacitance includes a polynomial function to describe the grading coefficient, γ. Using SPICE nomenclature, this can be expressed as:

$$C_d = C_{J0}\left(1-\frac{V_j}{VJ}\right)^{-\gamma(V_j)} \quad \text{Vj} \le \text{FC x VJ, or:}$$

$$C_d = C_{J0}(1-FC)^{-(1+\gamma(V_j))}\left(1-FC(1+\gamma(V_j))+\gamma(V_j)\frac{V_j}{VJ}\right) \quad \text{Vj} > \text{FC x VJ} \quad [1]$$

$$\gamma(V_j) = M + C_1 \cdot V_j + C_2 \cdot V_j^2 + C_3 \cdot V_j^3 \quad [2]$$

Where C_{J0} is the zero-bias capacitance, V_J is the junction potential, FC is the forward bias depletion capacitance coefficient (usually 0.5 for an abrupt junction), and V_J is the applied voltage across the diode. See Figure 22 for more details. The coefficients, C_1, C_2, and C_3 must be extracted for the non-linear model simulation. These can be extracted numerically, once a measurement of the capacitance curve as a function of voltage is available.

Nonetheless, upon inspection of equation [2], it is noted that the forth term of the polynomial contains a function of voltage raised to the third power. This polynomial in turn is the exponent of the capacitance equation [1]. For applied voltages that could exceed 20 Volts, the C_3 coefficient would have to be exceedingly small. In fact, it would likely have to be very accurately calculated as well. A small error when multiplied by a voltage raised to the third power, and then used as an exponent could cause severe convergence problems. It is proposed to set this coefficient to zero. By doing so, this allows a somewhat easier approach to solving for the remaining two coefficients. All that is needed is a capacitance ratio, and the voltage for which the ratio is determined. With this data, determining the coefficients becomes solving for two unknowns with two equations.

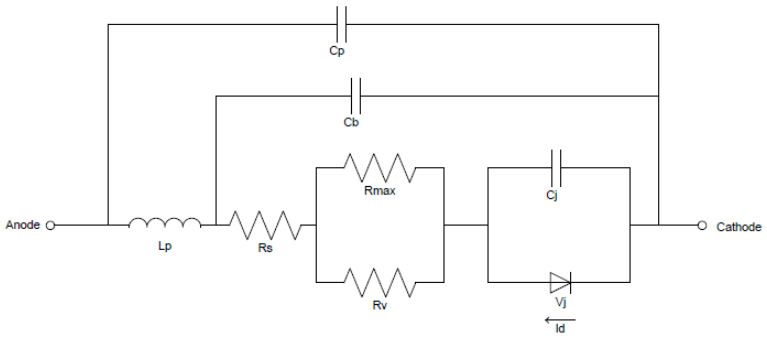


Figure 19: P-I-N Diode Model Diagram

As an example of this process, assume the following:

As $C(V_j)$ varies over the voltage range from $V_j = 0$ Volts to $V_j = -20$ Volts, the capacitance ratio drops by a factor of 0.5.

As $C(V_j)$ varies over the voltage range from $V_j = 0$ Volts to $V_j = -5$ Volts, the capacitance ratio drops by a factor of 0.647.

Setting the capacitance ratio to 0.5, VJ = 1.0, and M = 0.5:

$$\left(1-\frac{V_j}{VJ}\right)^{-\left(MV_j+C_1V_j^2+C_2V_j^3\right)} = 0.5 \ldots \text{ Substituting the above values:}$$

$$(1-(-20))^{-\left(0.5V_j+C_1V_j^2+C_2V_j^3\right)} = 0.5 \ldots \text{ Re-writing where } x = M + C_1 \cdot V_j + C_2 \cdot V_j^2$$

$$(21)^x = 0.5 \ldots \text{ Taking the logarithm of both sides of the equation:}$$

$$x \cdot \log(21) = \log(0.5) \ldots \text{ Solving for x:}$$

$$x \cong -0.227670249$$

Repeating the same procedure as above for $V_j = -5$ Volts, and a ratio of 0.647:

$$x \cong -0.242955642$$

With two equations, and two unknowns, C_1 and C_2 can be solved for:

$$-MV_{V_j=-20V} - C_1V_{V_j=-20V}^2 - C_2V_{V_j=-20V}^3 = -0.227670249$$
$$0.5(-20) + 400 \cdot C_1 - 8000 \cdot C_2 = -0.227670249$$

$$-MV_{V_j=-5V} - C_1V_{V_j=-5V}^2 - C_2V_{V_j=-5V}^3 = -0.242955642$$
$$0.5(-5) + 25 \cdot C_1 - 125 \cdot C_2 = -0.242955642$$

Re-written:

$$400 \cdot C_1 - 8000 \cdot C_2 \cong 10.227670248$$
$$25 \cdot C_1 - 125 \cdot C_2 \cong 2.742955642$$

Solving for C_1 and C_2:

$C_1 = 0.137767909$
$C_2 = 0.005609937$

For Further Reading:

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